LISTING OF THE CLAIMS

What is claimed is:

1. (Withdrawn) A method of producing a micro-electromechanical element comprising the following steps:

a) structuring a first intermediate layer, which is applied to a first main surface of a first semiconductor wafer, so as to produce a recess;

b) connecting the first semiconductor wafer via the first intermediate layer to a second semiconductor wafer in such a way that a hermetically sealed cavity is defined by the recess;

c) thinning one of the wafers from a surface facing layer away from said first intermediate so as to produce a diaphragm-like structure on top of the cavity;

d) producing electronic components in said thinned semiconductor wafer;

e) providing at least one further intermediate layer between the two semiconductor wafers, which, prior o the connection of the two semiconductor wafers, is structured, in such a way that the structure formed in said at least one further intermediate layer and the recess in said first intermediate layer define the cavity; and

f) producing at least one defined opening so as to provide access to the hermetically sealed cavity.

2. (Withdrawn) A method according to claim 1, wherein the main surface of the second semiconductor wafer, which is connected to the first semiconductor wafer via the intermediate layer, has applied thereto a second intermediate layer prior to the connecting step.

3. (Withdrawn) A method according to claim 2, wherein the second intermediate layer is structured in such a way that, after the connecting step, the structure formed in the second intermediate layer and the recess in the first intermediate layer define the cavity.

4. (Withdrawn) A method according to claim 1, wherein a cavity with areas of variable height is produced due to the use of a plurality of intermediate layers.

5. (Withdrawn) A method according to claim 1, wherein the first and the second wafer consist of silicon.

6. (Withdrawn) A method according to claim 1, wherein said plurality of intermediate layers consist of an oxide, a polysilicon, a nitride or of metal.

7. (Withdrawn) A method according to claim 1, wherein said intermediate layers are structured in such a way that, after the connection of the two wafers, a plurality of cavities is defined, said cavities being interconnected by channels and hermetically sealed from their surroundings.

8. (Withdrawn) A method according to claim 1, wherein the connection in step b) is carried out in a vacuum.

9. (Withdrawn) A method according to claim 1, wherein an SOI wafer is used as a first and/or second wafer.

10. (Withdrawn) A method according to claim 1, wherein said at least one defined opening is produced in the diaphragm-like structure.

11. (Withdrawn) A method according to claim 10, wherein said at least one defined opening is produced in the diaphragm-like structure by means of a needle, a blade, by the use of a pulsed laser radiation or by etching.

12. (Withdrawn) A method according to claim 7, wherein the channel is structured in the fashion of a labyrinth in step a) in such a way that disturbing products formed during the production of the opening are prevented from passing said channel.

13. (Withdrawn) A method of producing a micro-electromechanical element comprising the following steps:

a) structuring a first intermediate layer, which is applied to a first main surface of a first semiconductor wafer, so as to produce a recess;

b) connecting the first semiconductor wafer via the first intermediate layer to a second semiconductor wafer in such a way that a hermetically sealed cavity is defined by the recess;

c) thinning one of the wafers from a away from said first intermediate surface facing layer so as to produce a diaphragm-like structure on top of the cavity;

d) producing electronic components in said thinned semiconductor wafer; and

e) dicing a plurality of micro-electromechanical structures, which are formed in a wafer according to steps a) to d), so as to obtain chips, a defined opening, which provides access to the hermetically sealed

cavities, being produced by the dicing step.

14. (Withdrawn) A method according to claim 13, wherein the main surface of the second semiconductor wafer, which is connected to the first semiconductor wafer via the intermediate layer, has applied thereto a second intermediate layer prior to the connecting step.

15. (Withdrawn) A method according to claim 14, wherein the second intermediate layer is structured in such a way that, after the connecting step, the structure formed in the second intermediate layer and the recess in the first intermediate layer define the cavity.

16. (Withdrawn) A method according to claim 13, wherein a cavity with areas of variable height is produced due to the use of a plurality of intermediate layers.

17. (Withdrawn) A method according to claim 13, wherein the first and the second wafer consist of silicon.

18. (Withdrawn) A method according to claim 13, wherein said intermediate layer consist of an oxide, a polysilicon, a nitride or of metal.

19. (Withdrawn) A method according to claim 13, wherein said intermediate layers are structured in such a way that, after the connection of the two wafers, a plurality of cavities is defined, said cavities being interconnected by channels and hermetically sealed from their surroundings.

20. (Withdrawn) A method according to claim 13, wherein the connection in step b) is carried out in a vacuum.

21. (Withdrawn) A method according to claim 13, wherein an SOI wafer is used as a first and/or second wafer.

22. (Withdrawn) A method according to claim 19, wherein the channel is structured in the fashion of a labyrinth in step a) in such a way that disturbing products formed during the production of the opening are prevented from passing said channel.

23. (Previously submitted) A method of producing a micro-electromechanical element comprising the following steps:

a) structuring a first intermediate layer, which is applied to a first main surface of a first semiconductor wafer, so as to produce a recess;

b) connecting the first semiconductor wafer via the first intermediate layer to a second semiconductor wafer in such a way that a hermetically sealed cavity is defined by the recess;

c) thinning one of the wafers from a surface facing away from said first intermediate layer so as to produce a diaphragm-like structure on top of the cavity

d) producing electronic components in said thinned semiconductor wafer; wherein in step a) the intermediate layer is structured in such a way that, when the two wafers have been connected, at least two hermetically sealed cavities are defined, which are interconnected by a channel, a respective diaphragm-like structure being arranged on top of each of said cavities after step c),

and wherein the method additionally comprises the step e) of opening a defined opening through the diaphragm-like structure on top of one of the cavities.

24. (Previously Submitted) A method according to claim 23, wherein the main surface of the second semiconductor wafer, which is connected to the first semiconductor wafer via the intermediate layer, has applied thereto a second intermediate layer prior to the connecting step.

25. (Previously Submitted) A method according to claim 24, wherein the second intermediate layer is structured in such a way that, after the connecting step, the structure formed in the second intermediate layer and the recess in the first intermediate layer define the cavity.

26. (Previously Submitted) A method according to claim 23, wherein a cavity with areas of variable height is produced due to the use of a plurality of intermediate layers.

27. (Previously Submitted) A method according to claim 23, wherein the first and the second wafer consist of silicon.

28. (Previously Submitted) A method according to claim 23, wherein said intermediate layer consists of an oxide, a polysilicon, a nitride or of metal.

29. (Previously Submitted) A method according to claim 23, wherein the connection in step b) is carried out in a vacuum.

30. (Previously Submitted) A method according to claim 23, wherein an SOI wafer is used as a first and/or second wafer.

31. (Previously Submitted) A method according to claim 23, wherein said at least one defined opening is produced in the diaphragm-like structure by means of a needle, a blade, by the use of a pulsed laser radiation or by etching.

32. (Previously Submitted) A method according to claim 23, wherein the channel is structured in the fashion of a labyrinth in step a) in such a way that disturbing products formed during the production of the opening are prevented from passing said channel.

33. (Withdrawn) A method of producing a micro-electromechanical element comprising the following steps:

a) structuring a first intermediate layer, which is applied to a first main surface of a first semiconductor wafer, so as to produce a recess;

b) connecting the first semiconductor wafer via the first intermediate layer to a second semiconductor wafer in such a way that a hermetically sealed cavity is defined by the recess;

c) thinning one of the wafers from a surface facing away from said first intermediate layer so as to produce a diaphragm-like structure on top of the cavity;

d) producing electronic components in said thinned semiconductor wafer; and

e) producing a plurality of defined openings in the diaphragm-like structure in such a way that, when said openings have been produced, the diaphragm-like structure forms a supporting structure for the movable mass of an acceleration sensor.

34. (Withdrawn) A method according to claim 33, wherein the main surface of the second semiconductor wafer, which is connected to the first semiconductor wafer via the intermediate layer, has applied thereto a second intermediate layer prior to the connecting step.

35. (Withdrawn) A method according to claim 34, wherein the second intermediate layer is structured in such a way that, after the connecting step, the structure formed in the second intermediate layer and the recess in the first intermediate layer define the cavity.

36. (Withdrawn) A method according to claim 33, wherein a cavity with areas of variable height is produced due to the use of a plurality of intermediate layers.

37. (Withdrawn) A method according to claim 33, wherein the first and the second wafer consist of silicon.

38. (Withdrawn) A method according to claim 33, wherein said intermediate layer consists of an oxide, a polysilicon, a nitride or of metal.

39. (Withdrawn) A method according to claim 33, wherein the connection in step b) is carried out in a vacuum.

40. (Withdrawn) A method according to claim 33, wherein an SOI wafer is used as a first and/or second wafer.

41. (Withdrawn) A method according to claim 33, wherein said openings are produced in the diaphragm-like structure by means of a needle, a blade, by the use of a pulsed laser radiation or by etching.